line 25, change "contact" to --contacts--;

line 31, change "CLAIMS." to --WHAT IS CLAIMED IS:--.

IN THE CLAIMS:

Kindly claims 1 and 2. Kindly also amend claims 3-15, and add new claims 16-21, as follows:

3. (Amended) A semiconductor integrated circuit device, comprising:

a source region formed on a semiconductor substrate;

a first [conductive layer] conductor having a first resistivity formed [on] over said source region;

a first contact [hole] group having contacts connecting said source region and said first [conductive layer] conductor;

a second [conductive layer] conductor having a second resistivity [on] over said first [conductive layer] conductor;

a second contact [hole] group[, on an upper part of said source region,] having contacts connecting said first [conductive layer] conductor and said second [conductive layer] conductor;

a drain region formed on [a] said semiconductor substrate;

a third [conductive layer] conductor having said first resistivity formed [on] over said drain region;

a third contact [hole] group having contacts connecting said drain region and said third [conductive layer] conductor;

a fourth [conductive layer] conductor having said second resistivity formed [on] over said third [conductive layer] conductor;

a fourth contact [hole] group[, on an upper part of said drain region,] having contacts connecting said third [conductive layer] conductor and said fourth [conductive layer; wherein] conductor;

wherein a total number of [contact holes is respectively different between] contacts in said first contact [hole] group [and] is different from a total number of contacts in said [third] second contact [hole] group, and

a total number of [contact holes is respectively different between] contacts in said [second] third contact hole group [and] is different from a total number of contacts in said fourth contact [hole] group.

4. (Amended) The semiconductor integrated circuit device as [disclosed] claimed in claim 3, wherein the total number of [contact holes] contacts in said first contact [hole] group is the same as the total number of [contact holes] contacts in said third contact [hole] group, and the total number of [contact holes] contacts in said second contact [hole] group is the same as the total number of [contact holes] contacts in said fourth contact [hole] group.

5. (Amended) The semiconductor integrated circuit device as [disclosed] claimed in claim 4, wherein said fist resistivity is higher than said second resistivity, [the] and a total number of [contact holes for] contacts in said first contact [hole] group and in said third contact [hole] group is [more] greater than [the] a total number of [contact holes for] contacts in said second contact [hole] group and in said fourth contact [hole] group.

6. (Amended) A semiconductor integrated circuit device, comprising:

a first impurity diffusion region and a second impurity diffusion region formed on a semiconductor substrate, extending in a first direction and standing side by side in a second direction;

a first [conductive layer] conductor having a first resistivity formed [on] over said first impurity diffusion region;

a first contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said first direction, for connecting said first impurity diffusion region and said first [conductive layer] conductor;

a second [conductive layer] conductor having a second resistivity formed [on] over said first [conductive layer] conductor;

a second contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said first direction, for connecting said first [conductive layer] conductor and said second [conductive layer, at an upper part of said first impurity diffusion region] conductor;

a third [conductive layer] conductor having said first resistivity formed [on] over said second impurity diffusion region;

a third contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said first direction, for connecting said second impurity diffusion region and said third [conductive layer] conductor;

a fourth [conductive layer] conductor having said second resistivity formed [on] over said third [first conductive layer] conductor; and

a fourth contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said first direction, for connecting said third [conductive layer] conductor and said fourth [conductive layer, at an upper part of said second impurity diffusion region, wherein] conductor,

wherein said first contact [hole] group is arranged between neighboring [contact holes] contacts of said second contact [hole] group, and

wherein said third contact [hole] group is arranged between neighboring [contact holes] contacts of said fourth contact [hole] group.

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7. (Amended) The semiconductor integrated circuit device as [disclosed] claimed in claim 6, wherein

a distance between a contact [hole] of said first contact group and a contact [hole] of said second contact [hole] group adjacent to the contact [hole] of said first contact [hole] group is a fixed value, and

a distance between a contact [hole] of said third contact group and a contact [hole] of said fourth contact [hole] group adjacent to the contact [hole] of said third contact [hole] group is a fixed value.

8. (Amended) The semiconductor integrated circuit device as [disclosed] claimed in claim 6, wherein

an interval between [contact holes] contacts of said first contact group situated between neighboring [holes] contacts of said second contact [hole] group is a fixed value, and

an interval between [contact holes] contacts of said third contact group situated between neighboring [holes] contacts of said fourth contact [hole] group is a fixed value.

(Amended) The semiconductor integrated circuit device as [disclosed] claimed in claim 6, wherein

said first impurity diffusion region has

a first side and a second side running in said second direction,

a third side running in said first direction and opposite to said second impurity diffusion region,

a first distance defined as a distance from said first side to an edge of said first contact [hole] group extremely close to said first side,

a second distance defined as a distance from said second side to an edge of said first contact [hole] group extremely close to said second side, and

a third distance defined as a distance from said third side to an edge of said first contact hole group extremely close to said third side,

said second impurity diffusion region has

a fourth side and a fifth side running in said second direction,

a sixth side running in said first direction and opposite to said first impurity diffusion region,

a fourth distance defined as a distance from said fourth side to an edge of said third contact [hole] group extremely close to said fourth side,

a fifth distance defined as a distance from said fifth side to an edge of said third contact [hole] group extremely close to said fifth side, and

a sixth distance defined as a distance from said sixth side to an edge of said third contact [hole] group extremely close to said sixth side, [wherein]

said first distance and said second distance are both larger than said third distance, and said fourth distance and said fifth distance are both larger than said sixth distance.

10. (Amended) The semiconductor integrated circuit device as [disclosed] claimed in claim 6, wherein

said first contact [hole] group is divided into a plurality of subgroups [according to] each having a predetermined fixed number of [contact holes] contacts, and each subgroup is arranged between adjacent [contact holes] contacts of said second contact [hole] group, and

said third contact [hole groups are] group is divided into a plurality of subgroups [according to] each having a predetermined fixed number of [contact holes,] contacts, and each subgroup is arranged between adjacent [contact holes] contacts of said fourth contact [hole] group.

11. (Amended) the semiconductor integrated circuit device as [disclosed] claimed in claim 10, wherein

a distance from [contact holes] contacts of said first contact [hole] group and [contact holes] contacts of said second contact [hole] group adjacent to [holes] contacts of said first contact [hole] group, has a fixed value, and

a distance from [contact holes] contacts of said third contact [hole] group and [contact holes] contacts of said fourth contact [hole] group adjacent ot [holes] contacts of said third contact [hole] group, has a fixed value.

12. (Amended) The semiconductor integrated circuit device as [disclosed] claimed in claim 10, wherein

an interval between [contact holes] contacts of said first contact [hole groups] group arranged between adjacent [contact holes] contacts of said second contact [hole] group has a fixed value, and

an interval between [contact holes] contacts of said third contact [hole groups] group arranged between adjacent [contact holes] contacts of said fourth contact [hole] group has a fixed value.

94 13. (Amended) The semiconductor integrated circuit device as [disclosed] claimed in claim 8, wherein

said first impurity diffusion region has

a first side and a second side running in said second direction,

a third side running in said first direction and opposite to said second impurity diffusion region,

a first distance defined as a distance from said first side to an edge of said first contact [hole] group extremely close to said first side,

a second distance defined as a distance from said second side to an edge of said first contact [hole] group extremely close to said second side, and

a third distance defined as a distance from said third side to an edge of said first contact hole group extremely close to said third side,

said second impurity diffusion region has

a fourth side and a fifth side running in said second direction,

a sixth side running in said first direction and opposite to said first impurity diffusion region,

a fourth distance defined as distance from said fourth side to an edge of said third contact [hole] group extremely close to said fourth side,

a fifth distance defined as a distance from said fifth side to an edge of said third contact [hole] group extremely close to said fifth side, and

a sixth distance defined as a distance from said sixth side to an edge of said third contact [hole] group extremely close to said sixth side, [wherein] said first distance and said second distance are both larger than said third distance, and said fourth distance and said fifth distance are both larger than said sixth distance.

14. (Amended) A semiconductor integrated circuit, comprising a first transistor for input and a second transistor for output, said first transistor and said second transistor being connected to an input/output terminal, wherein

said first transistor [comprising:] includes

a first impurity diffusion region and a second impurity diffusion region formed on a semiconductor substrate, extending in a first direction and standing side by side in a second direction;

a first [conductive layer] conductor having a first resistivity formed [on] over said first impurity diffusion region;

a first contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said first direction, for connecting said first impurity diffusion region and said first [conductive layer] conductor;

a second [conductive layer] conductor having a second resistivity formed [on] over said first [conductive layer] conductor;

a second contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said first direction, for connecting said first [conductive layer] conductor and said second [conductive layer, at an upper part of said first impurity diffusion region] conductor;

a third [conductive layer] conductor having said first resistivity formed [on] over said second impurity diffusion region;

a third contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said first direction, for connecting said second impurity diffusion region and said third [conductive layer] conductor;

a fourth [conductive layer] conductor having said second resistivity formed [on] over said third [first conductive layer] conductor; and

a fourth contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said first direction, for connecting said third [conductive layer] conductor and said fourth [conductive layer, at an upper part of said second impurity diffusion region, wherein] conductor,

said first contact [hole] group has a predetermined fixed number of [contact holes] contacts arranged between each neighboring contact [hole] of said second contact [hole] group, and has a first fixed interval between said predetermined number of arranged [contact holes] contacts and adjacent [contact holes, and] contacts

said third contact [hole] group has a predetermined fixed number of [contact holes] contacts arranged between each neighboring contact [hole] of said fourth contact [hole] group, and has said first fixed interval between said predetermined number of arranged [contact holes] contacts and adjacent [contact holes, and] contacts,

said second transistor includes

a third impurity diffusion region and a fourth impurity diffusion region formed on [a] said semiconductor substrate, extending in a third direction and standing side by side in a fourth direction;

a fifth [conductive layer] conductor having [a] said first resistivity formed [on] over said third impurity diffusion region;

a fifth contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said third direction, for connecting said third impurity diffusion region and said fifth [conductive layer] conductor;

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a sixth [conductive layer] conductor having [a] said second resistivity formed [on] over said fifth [conductive layer] conductor;

a sixth contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said third direction, for connecting said fifth [conductive layer] conductor and said sixth [conductive layer, at an upper part of said third impurity diffusion region] conductor;

a seventh [conductive layer] conductor having said first resistivity formed [on] over said fourth impurity diffusion region;

a seventh contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said third direction, for connecting said fourth impurity diffusion region and said seventh [conductive layer] conductor;

an eighth [conductive layer] conductor having said second resistivity formed [on] over said seventh [first conductive layer] conductor; and

an eighth contact [hole] group, having a plurality of [contact holes] contacts arranged side by side in said third direction, for connecting said seventh [conductive layer] conductor and said eighth [conductive layer, at an upper part of said fourth impurity diffusion region, wherein] conductor,

said fifth contact [hole] group has a predetermined fixed number of [contact holes] contacts arranged between each neighboring contact [hole] of said sixth contact [hole] group, and has said first fixed interval between said predetermined number of arranged [contact holes] contacts and adjacent [contact holes] contacts, and

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said seventh contact [hole] group has a predetermined fixed number of [contact holes] contacts arranged between each neighboring contact [hole] of said eighth contact [hole] group, and has said first fixed interval between said predetermined number of arranged [contact holes] contacts and adjacent [contact holes] contacts.

15. (Amended) The semiconductor integrated circuit as [disclosed] claimed in claim 14, having

a first side, for said first impurity diffusion region, running in said first direction and opposite to said second impurity diffusion region;

a second side, for said second impurity diffusion region, running in said first direction and opposite to said first impurity diffusion region;

a third side, for said third impurity diffusion region, running in said third direction and opposite to said fourth impurity diffusion region;

a fourth side, for said fourth impurity diffusion region, running in said third direction and opposite to said third impurity diffusion region;

a first distance defined as a distance between said first side and said second side; and

a second distance defined as a distance between said third side and said fourth side,

94 [wherein]

wherein said first distance and said second distance are equal.

--16. A transistor for use in an input protection circuit that protects circuitry fabricated on a semiconductor substrate, said transistor comprising:

a source region formed on the semiconductor substrate;

a first conductor having a first resistance formed over the source region;

95 a first number of first contacts connecting said source region and said first conductor;

a second conductor having a second resistance which is lower than the first resistance, said second conductor being formed over said first conductor;

a second number of second contacts connecting said first and second conductors;

a drain region formed on the semiconductor substrate;

a third conductor having the first resistance formed over the drain region;

a third number of third contacts connecting said drain region and said third conductor;

a fourth conductor having the second resistance formed over said third conductor;

a fourth number of fourth contacts connecting said third and fourth conductors;

a gate insulating layer formed on the semiconductor substrate between said source and drain regions; and

a gate electrode formed on the gate insulating layer,

wherein the first number is more than twice as large as the second number, and

wherein the third number is more than twice as large as the fourth number.

17. A transistor according to claim 16, wherein the first number is equal to the third number and the second number is equal to the fourth number.

18. A transistor according to claim 16, wherein said second contacts are located over end portions of said source region and said first contacts holes are located over a central portion of said source region.

19. A transistor according to claim 16, wherein said fourth contacts are located over end portions of said drain region and said third contacts are located over a central portion of said drain region.

20. A transistor according to claim 16, wherein a distance from an end of the source region to a nearest one of the first contacts is equal to one or greater than a distance from the gate electrode to said nearest one of the first contacts.

21. A transistor according to claim 16, wherein a distance from an end of the drain region to a nearest one of the third contacts is equal to or greater than a distance from the gate electrode to said nearest one of the third contacts.--

IN THE ABSTRACT:

Please replace the present abstract (on page 18 of the application) with the new abstract that is attached to this Amendment on a separate page.